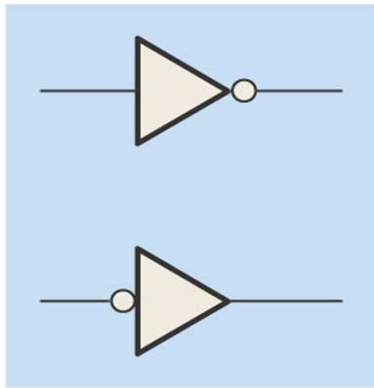
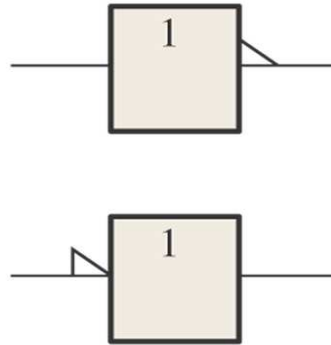


Figure 3-1 Standard logic symbols for the inverter (ANSI/IEEE Std. 91-1984).



(a) Distinctive shape symbols with negation indicators



(b) Rectangular outline symbols with polarity indicators

Figure 3-2 Inverter operation with a pulse input. Open file F03-02 to verify inverter operation.

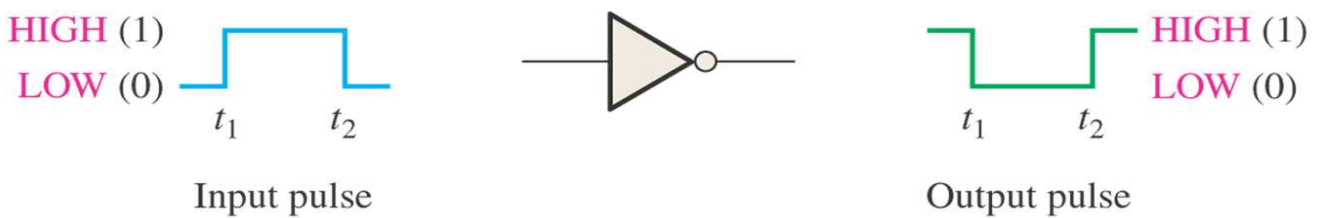


Figure 3-3 Timing diagram for the case in Figure 3-2.

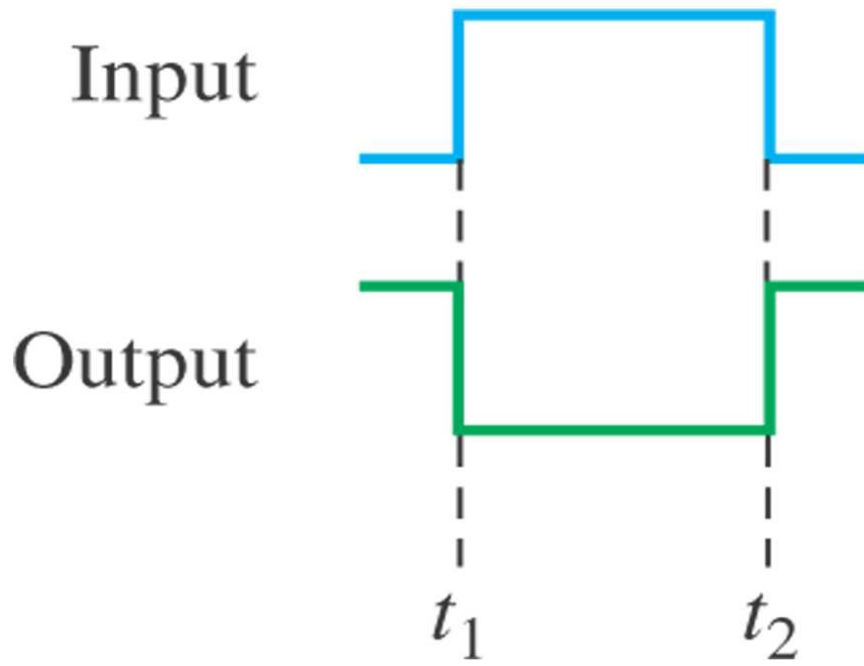


Figure 3-4

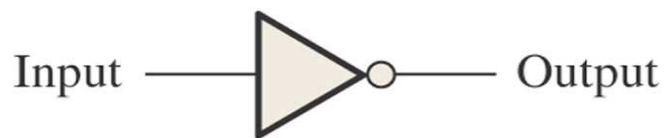


Figure 3-5

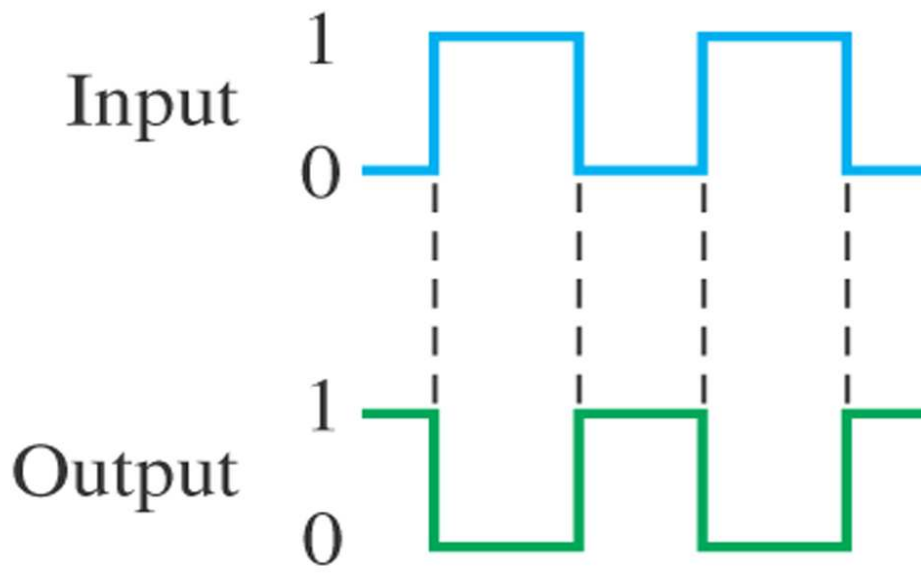


Figure 3-6 The inverter complements an input variable.

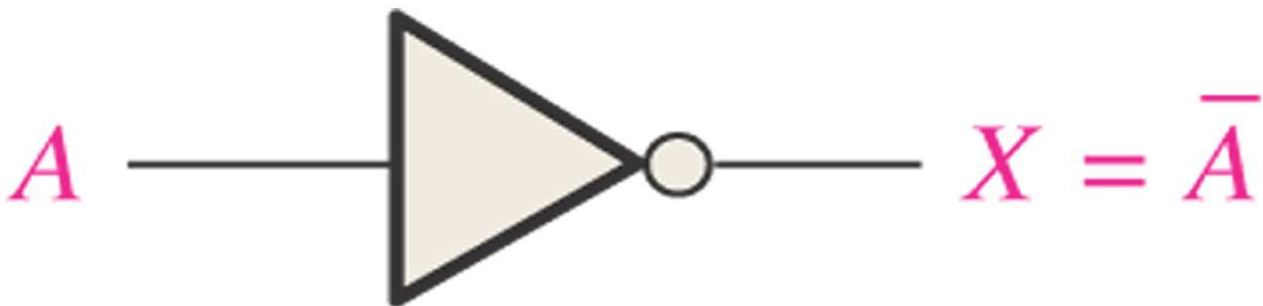
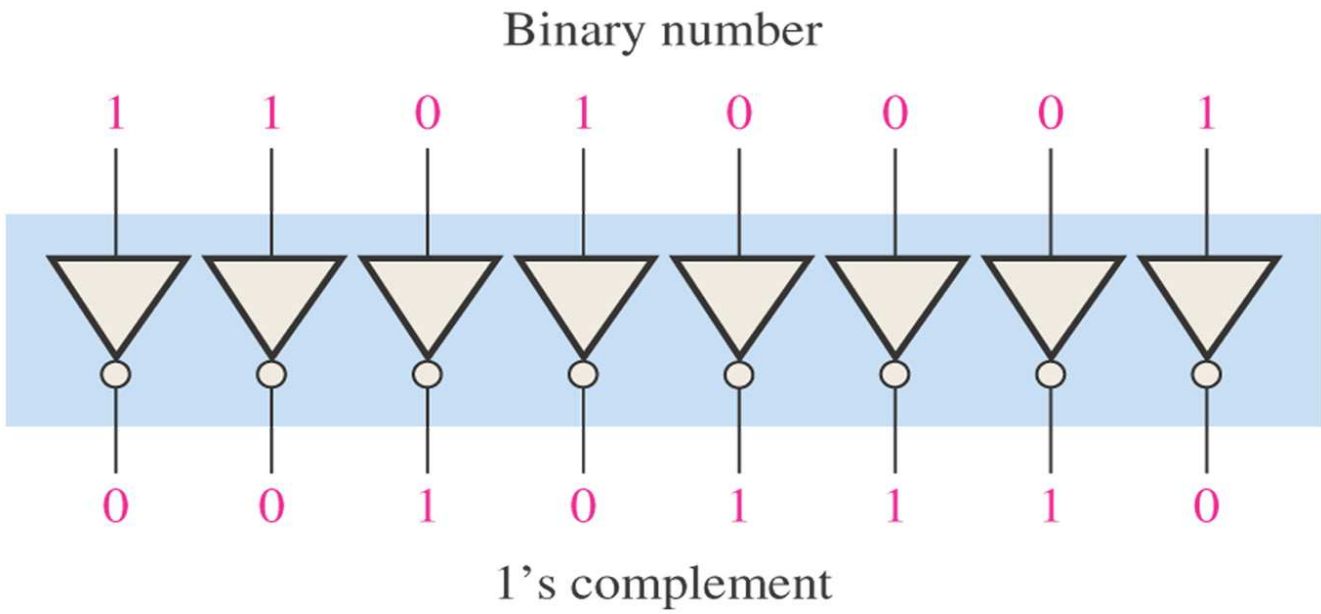


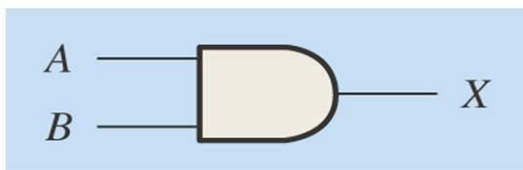
Figure 3-7 Example of a 1's complement circuit using inverters.



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Figure 3-8 Standard logic symbols for the AND gate showing two inputs (ANSI/IEEE Std. 91-1984).



(a) Distinctive shape



(b) Rectangular outline with the AND (&) qualifying symbol

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Figure 3-9 All possible logic levels for a 2-input AND gate. Open file F03-09 to verify AND gate operation.

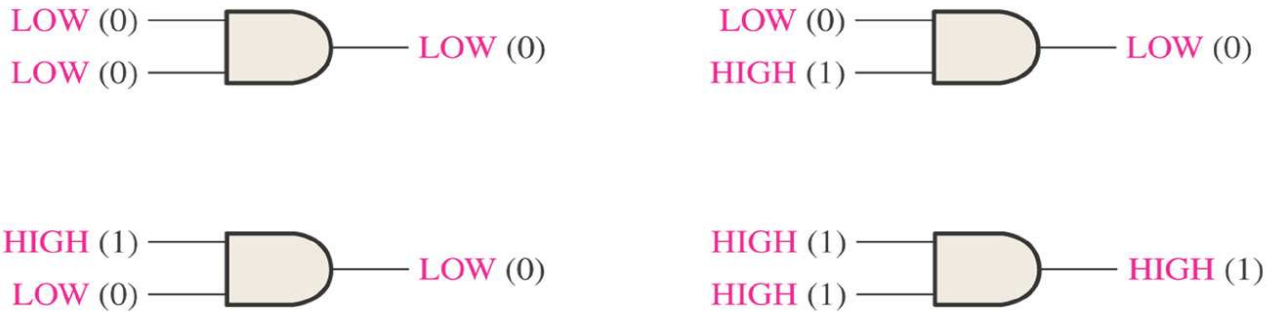


Figure 3-10 Example of AND gate operation with a timing diagram showing input and output relationships.

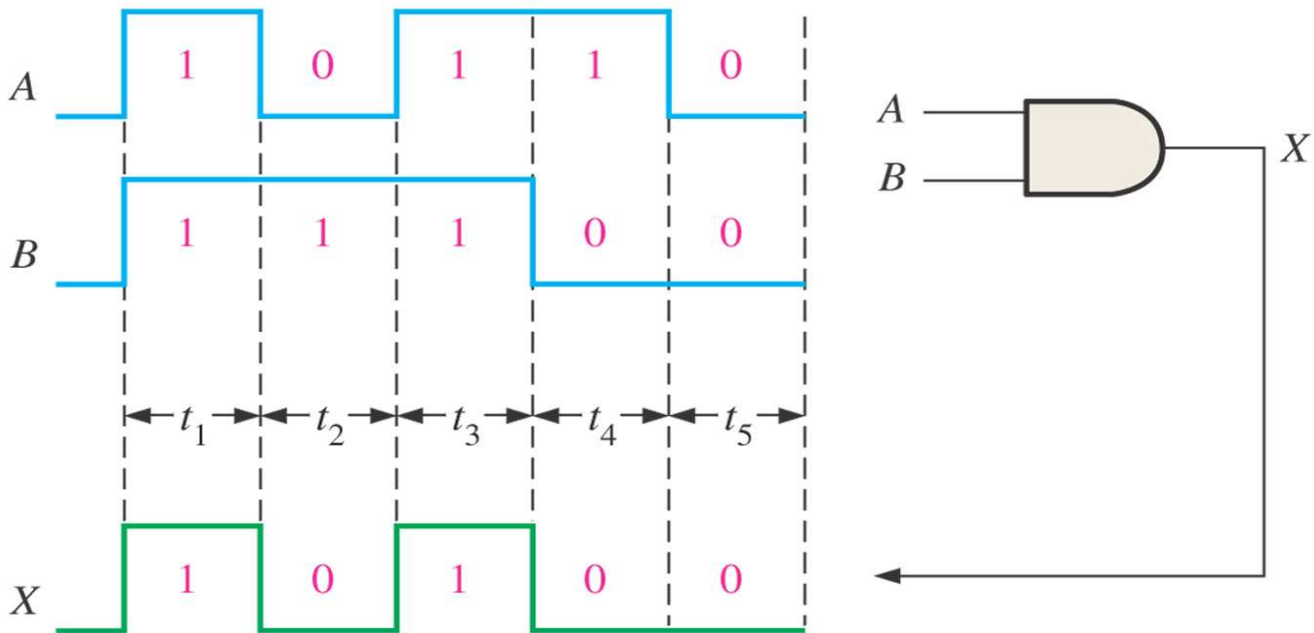
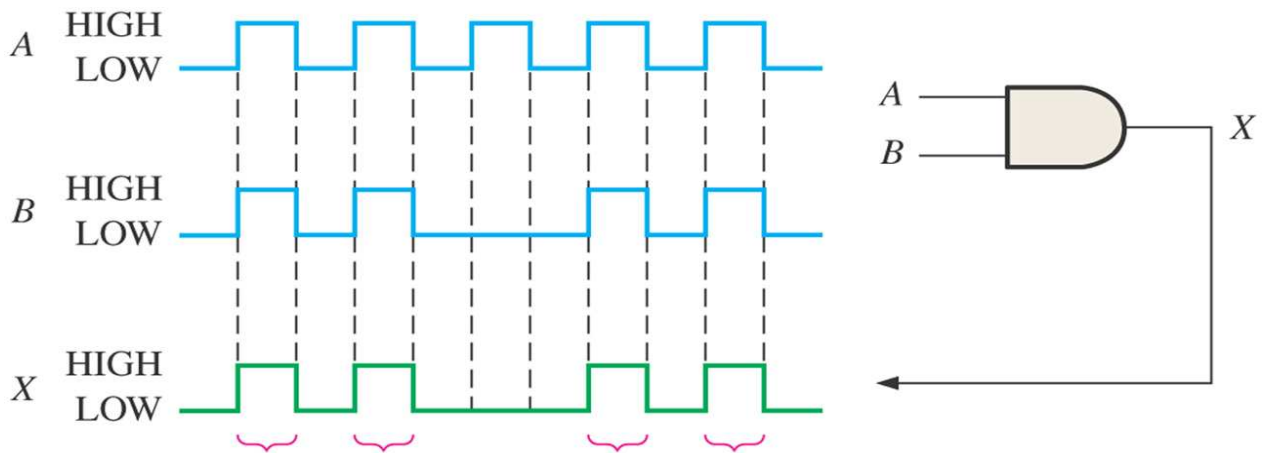


Figure 3-11



A and B are both HIGH during these four time intervals.
Therefore X is HIGH.

Figure 3-12

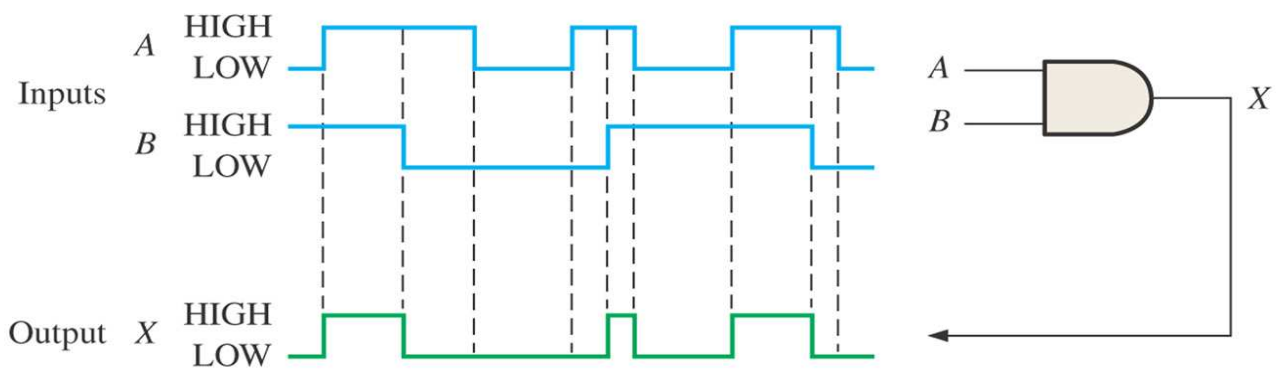


Figure 3-13

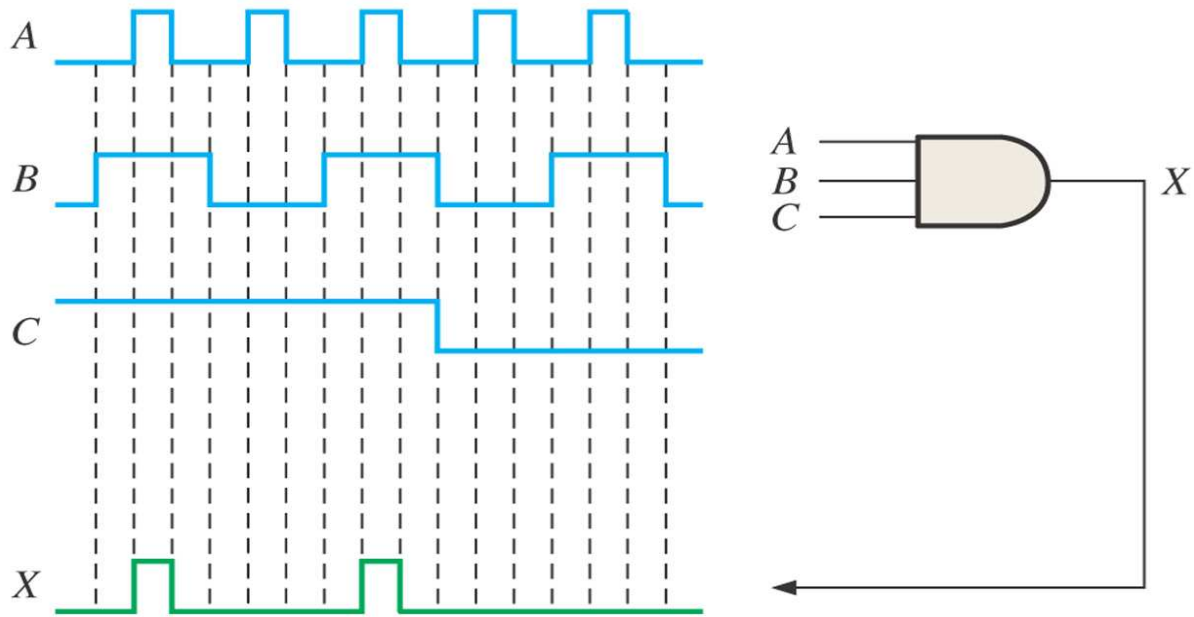
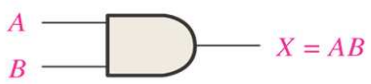
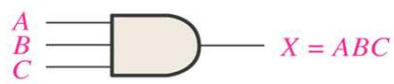


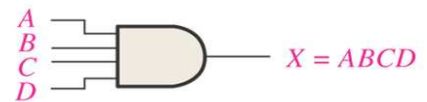
Figure 3-14 Boolean expressions for AND gates with two, three, and four inputs.



(a)



(b)



(c)

Figure 3-15 An AND gate performing an enable/inhibit function for a frequency counter.

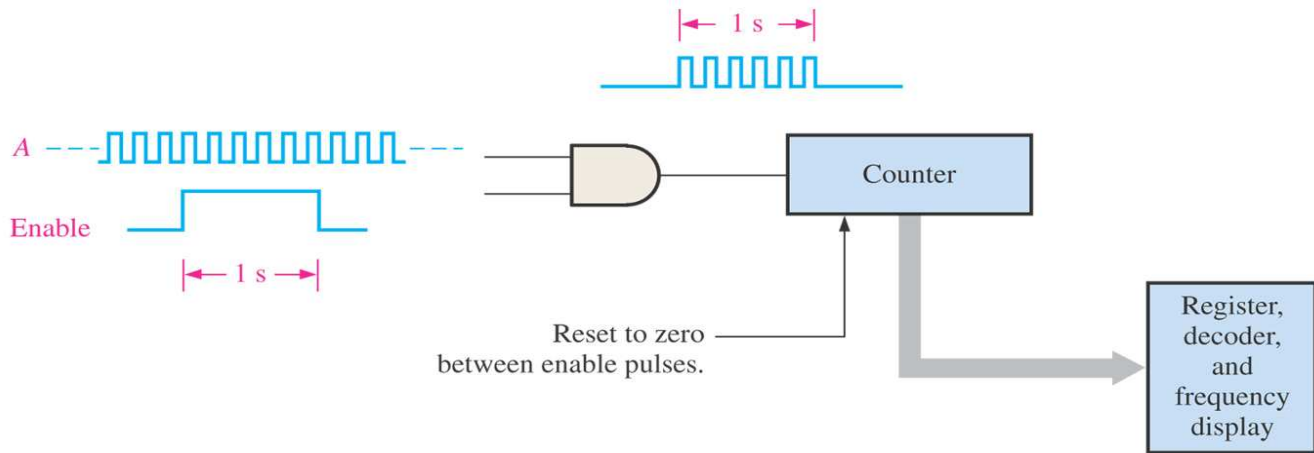


Figure 3-16 A simple seat belt alarm circuit using an AND gate.

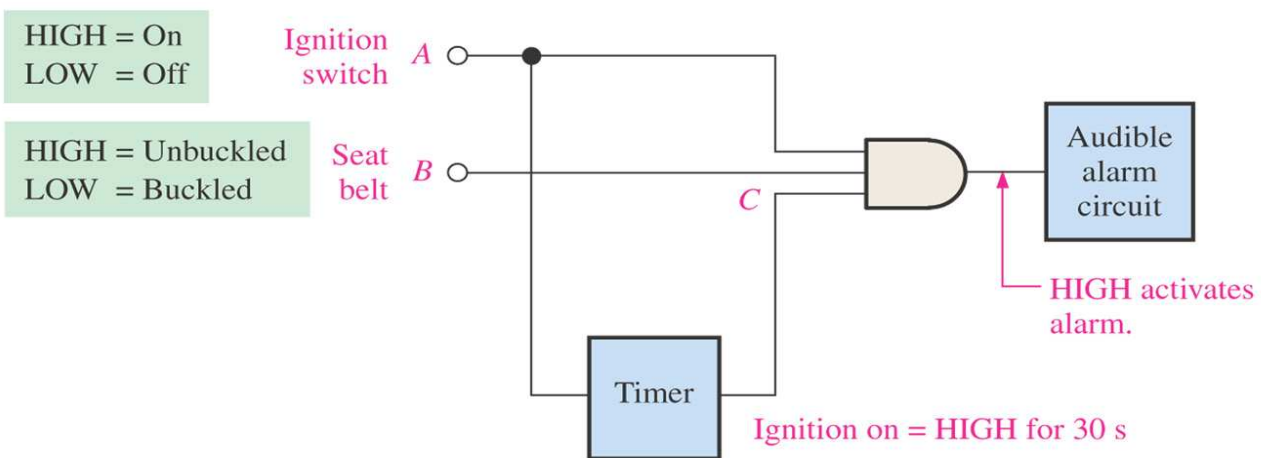
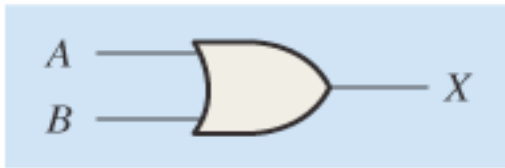
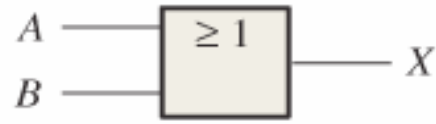


Figure 3-17 Standard logic symbols for the OR gate showing two inputs (ANSI/IEEE Std. 91-1984).



(a) Distinctive shape



(b) Rectangular outline with the OR (≥ 1) qualifying symbol

Figure 3-18 All possible logic levels for a 2-input OR gate. Open file F03-18 to verify OR gate operation.

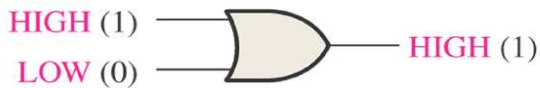
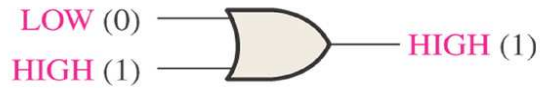
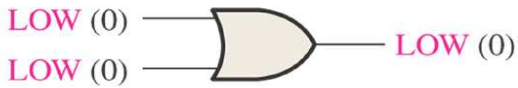


Figure 3-19 Example of OR gate operation with a timing diagram showing input and output time relationships.

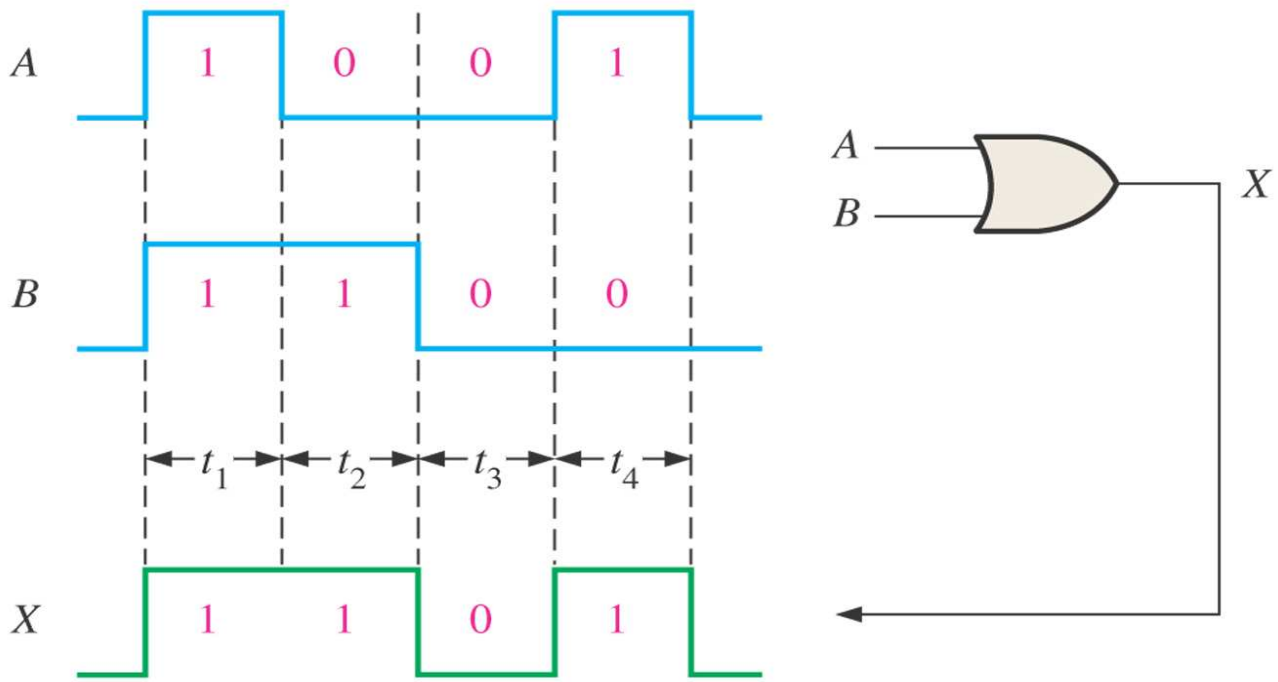
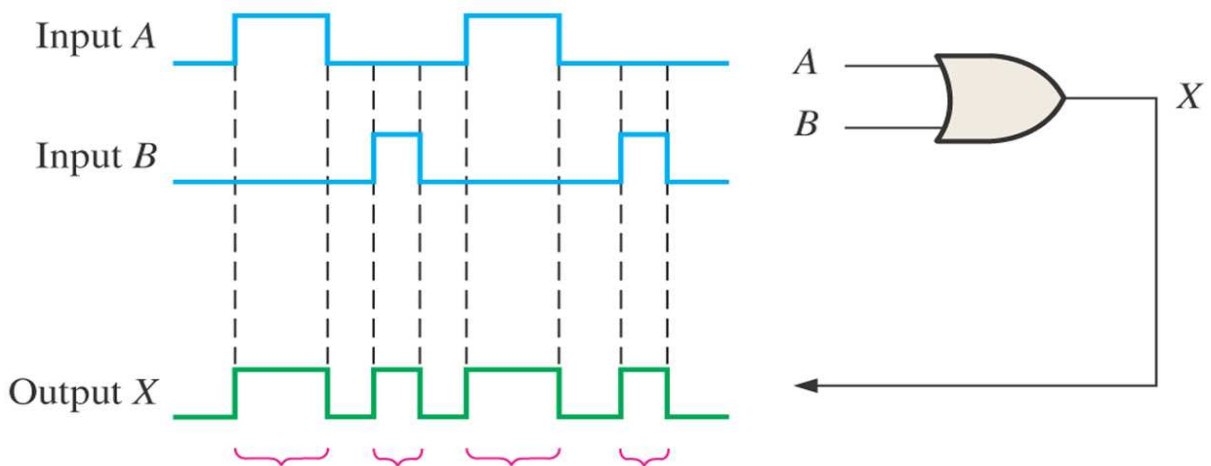


Figure 3-20



When either input or both inputs are HIGH,
the output is HIGH.

Figure 3-21

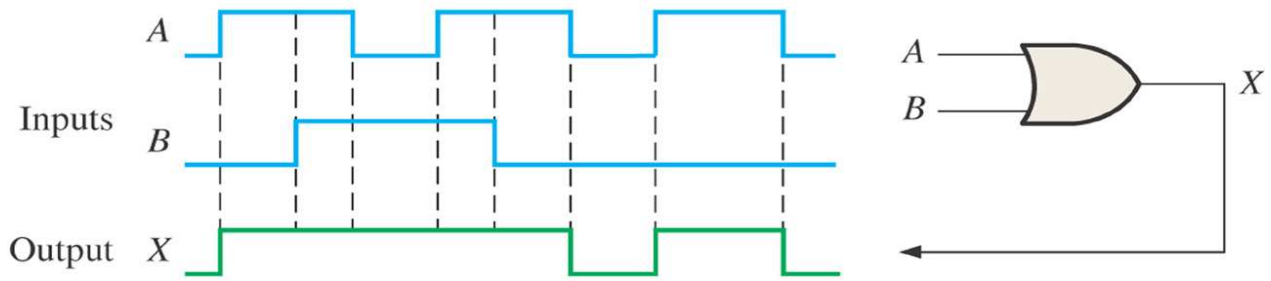


Figure 3-22

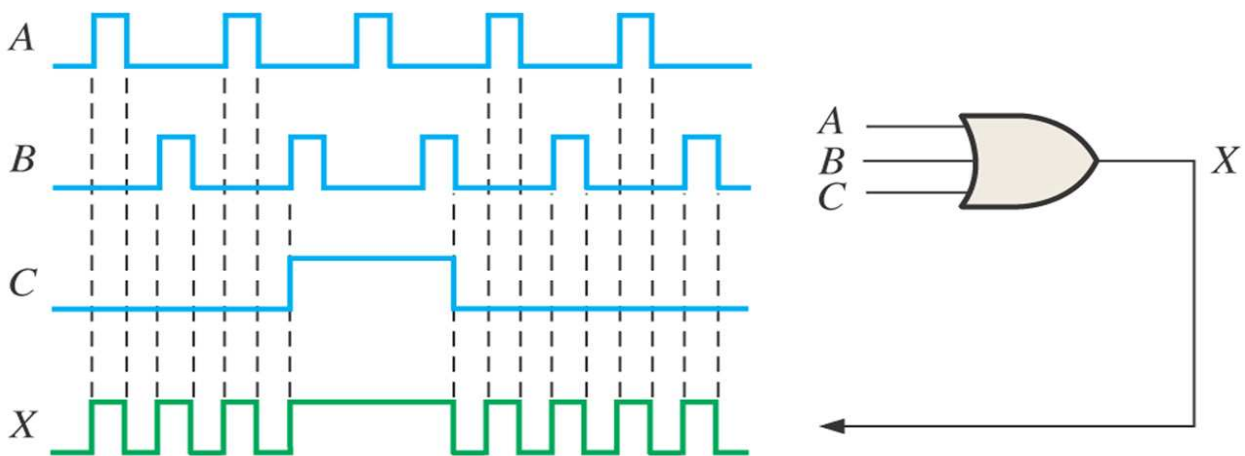


Figure 3–23 Boolean expressions for OR gates with two, three, and four inputs.

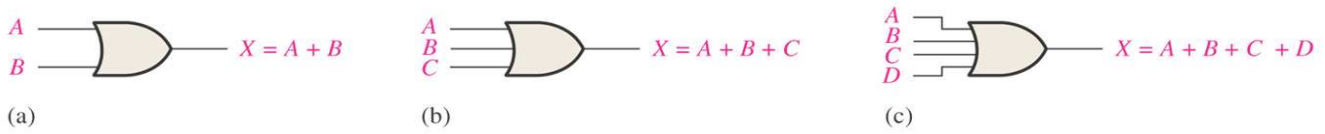


Figure 3–24 A simplified intrusion detection system using an OR gate.

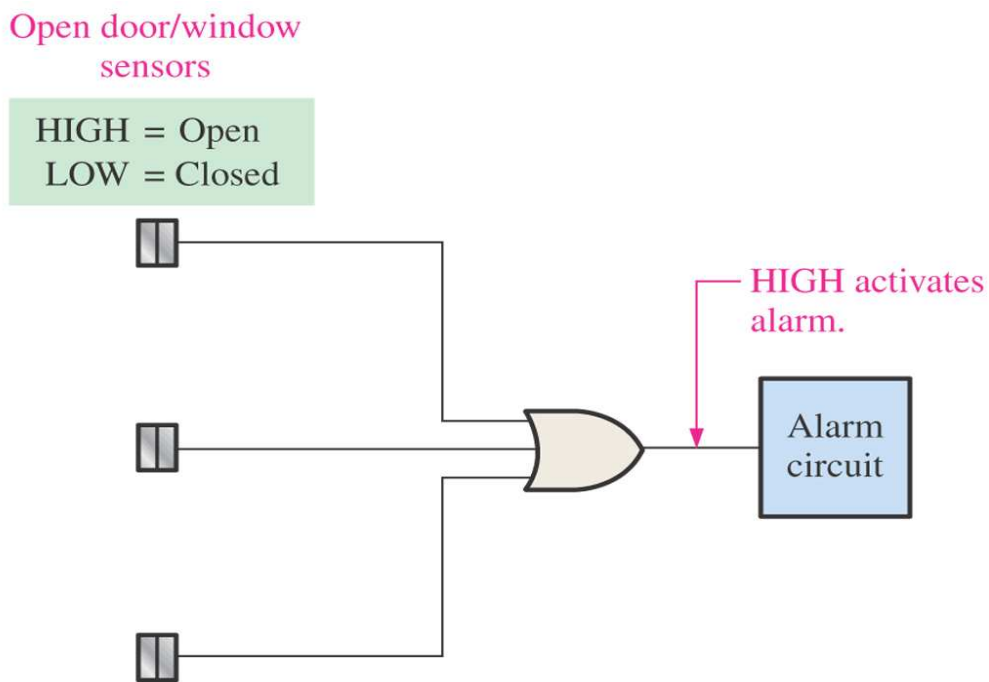


Figure 3–25 Standard NAND gate logic symbols (ANSI/IEEE Std. 91-1984).

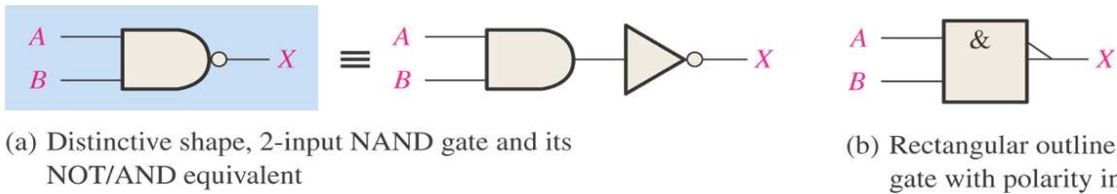


Figure 3–26 Operation of a 2-input NAND gate. Open file F03-26 to verify NAND gate operation.

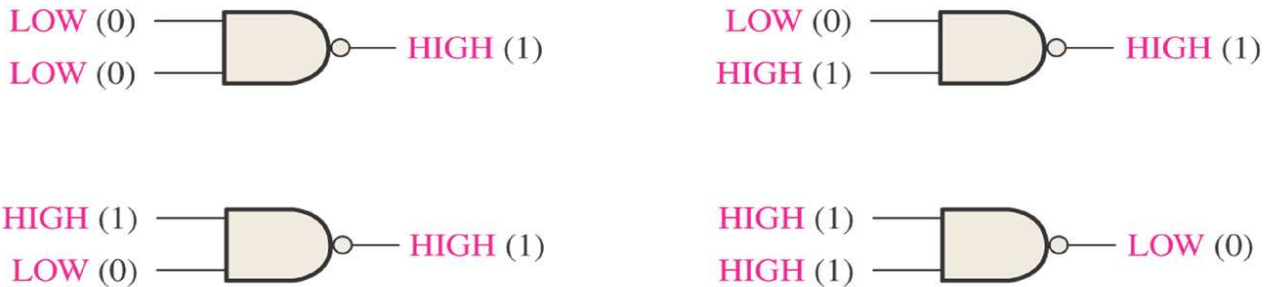
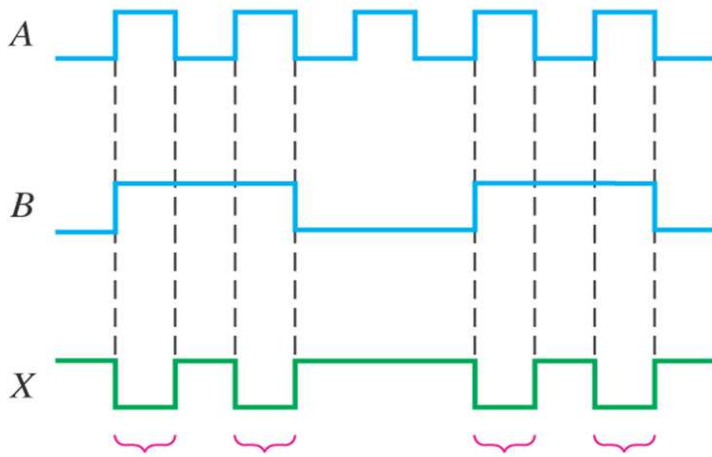


Figure 3-27



A and B are both HIGH during these four time intervals. Therefore X is LOW.

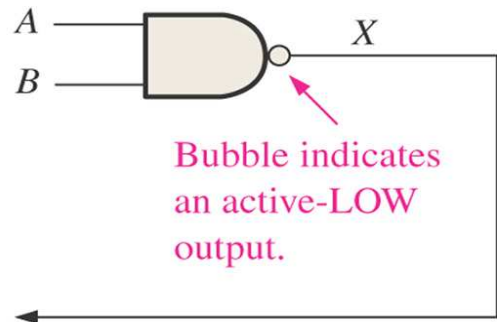


Figure 3-28

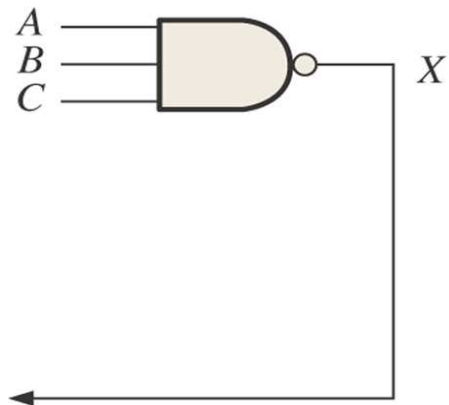
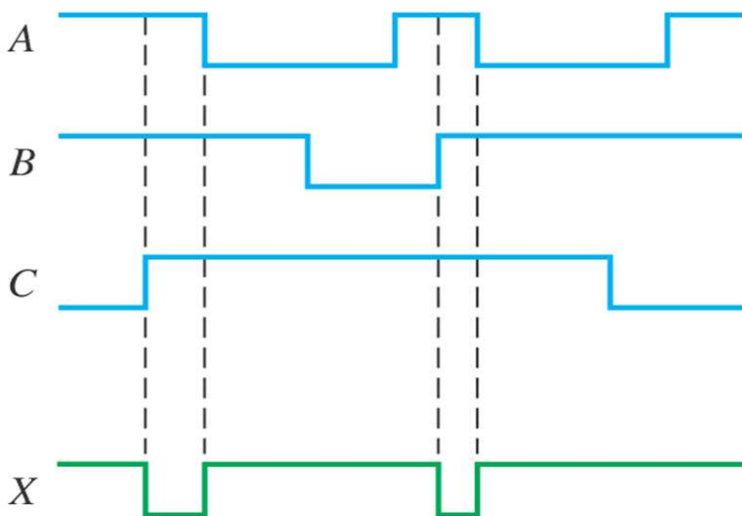


Figure 3–29 Standard symbols representing the two equivalent operations of a NAND gate.

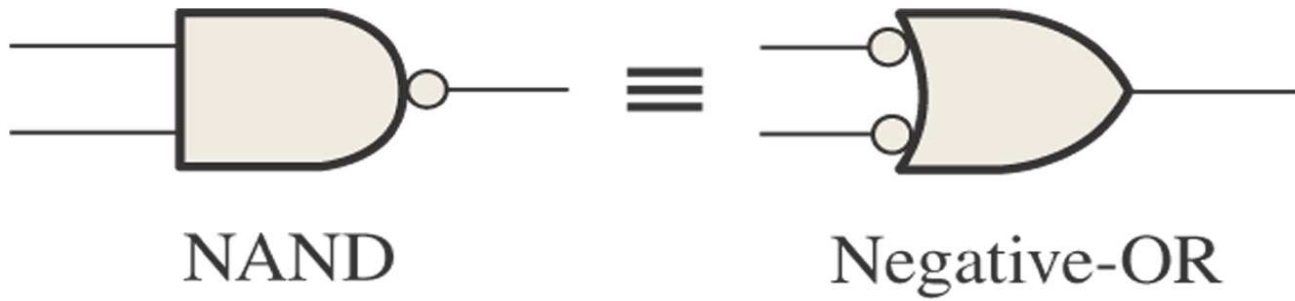


Figure 3–30

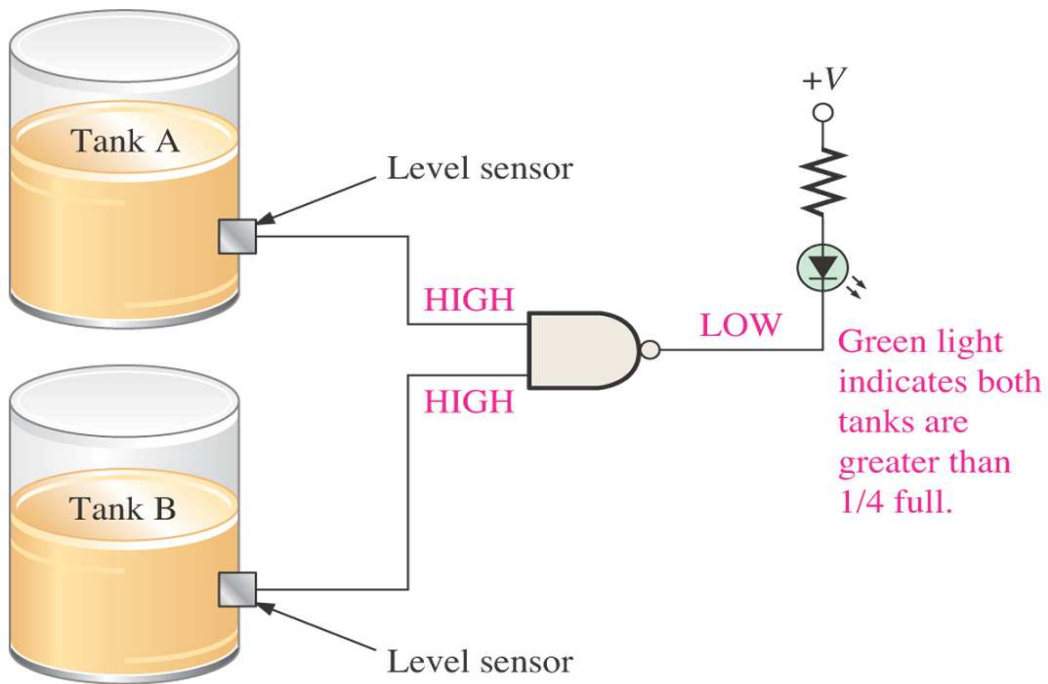


Figure 3-31

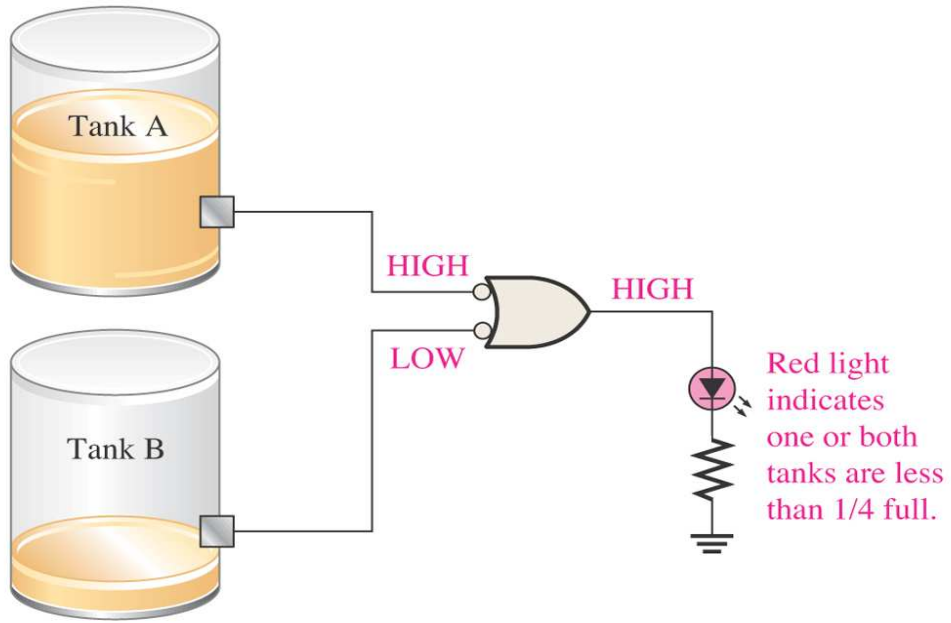


Figure 3-32

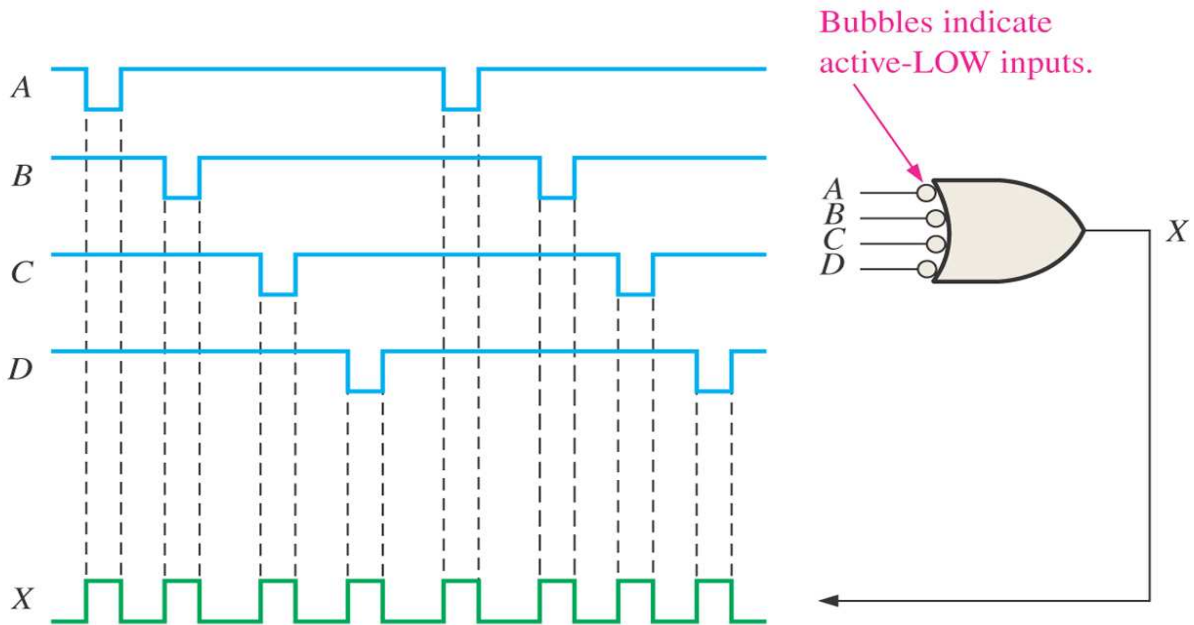


Figure 3-33 Standard NOR gate logic symbols (ANSI/IEEE Std. 91-1984).

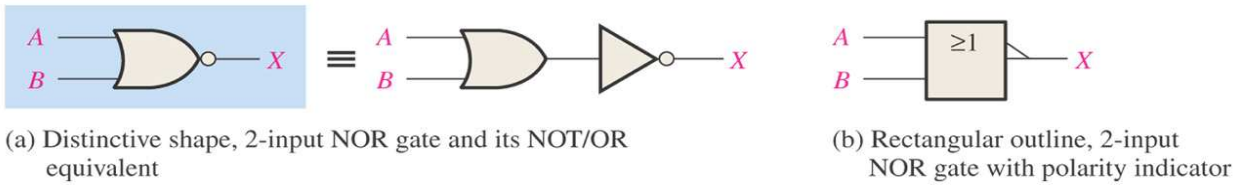


Figure 3-34 Operation of a 2-input NOR gate. Open file F03-34 to verify NOR gate operation.

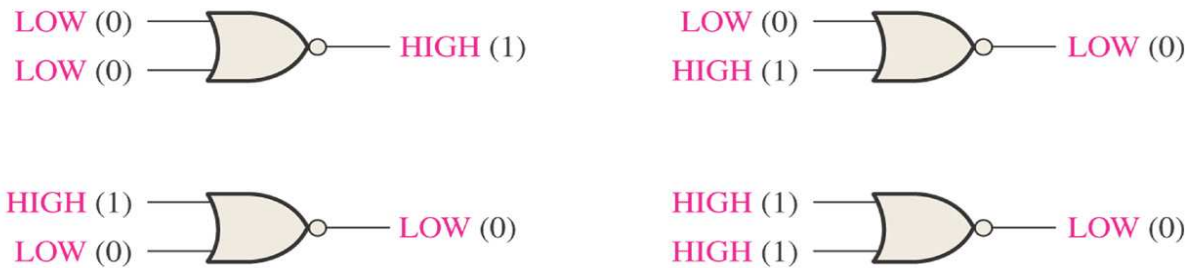
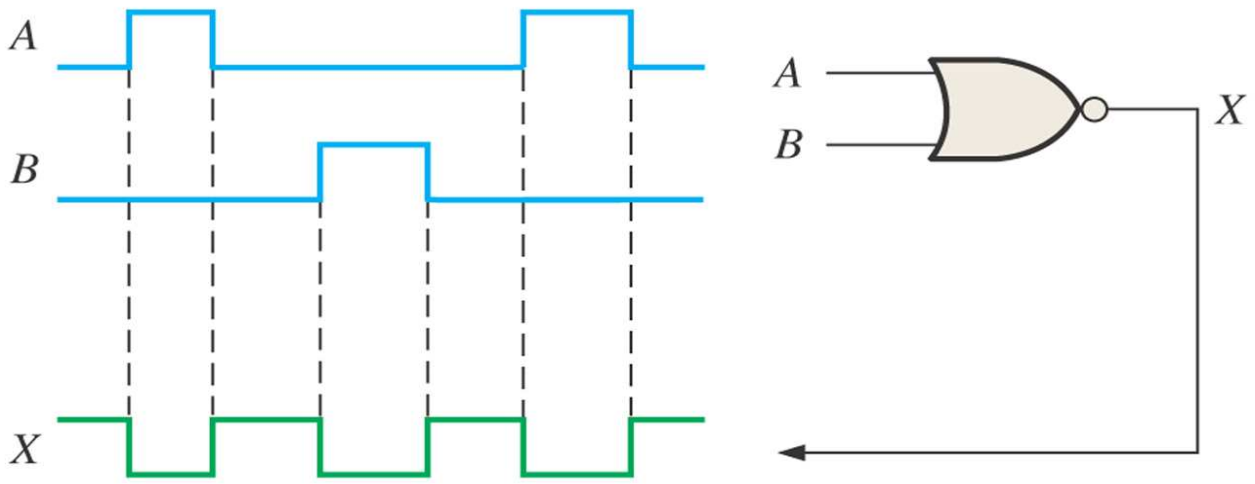


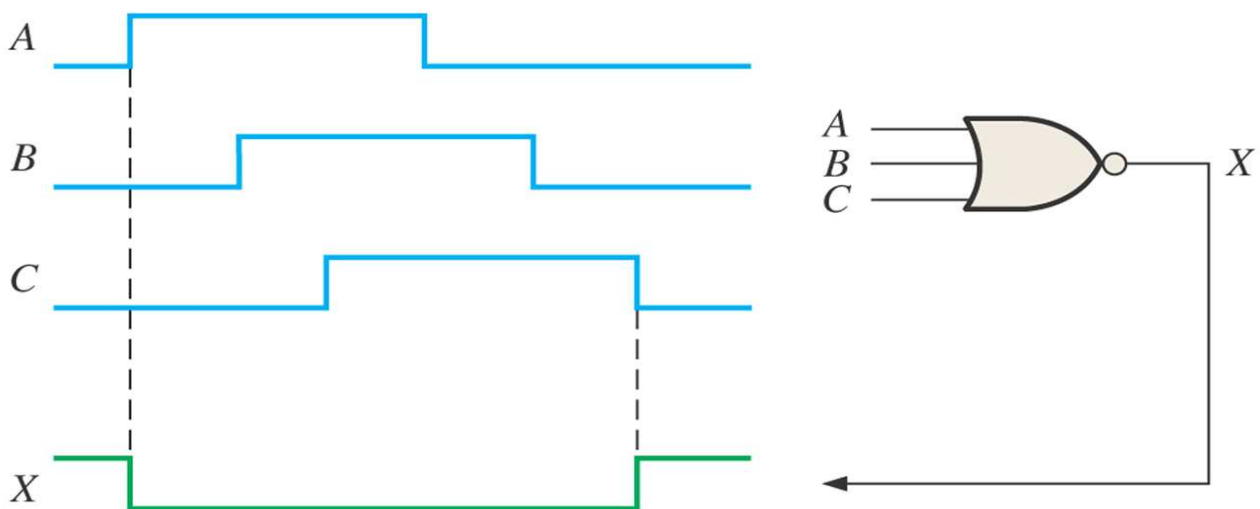
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Figure 3–37 Standard symbols representing the two equivalent operations of a NOR gate.

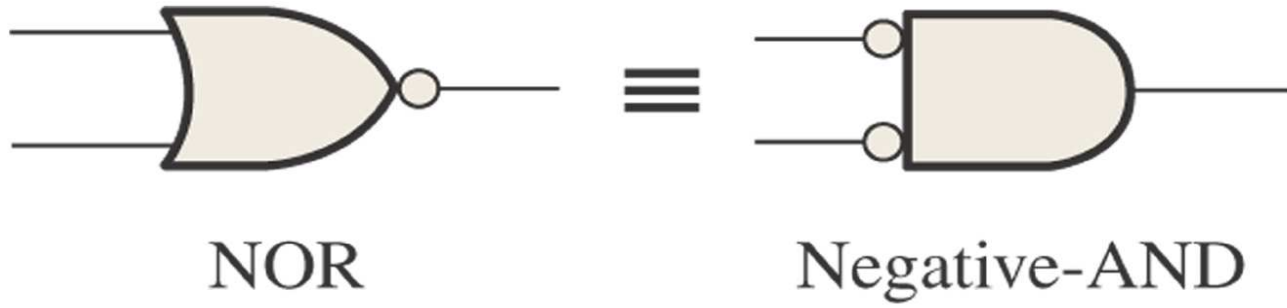


Figure 3–38



Figure 3-39

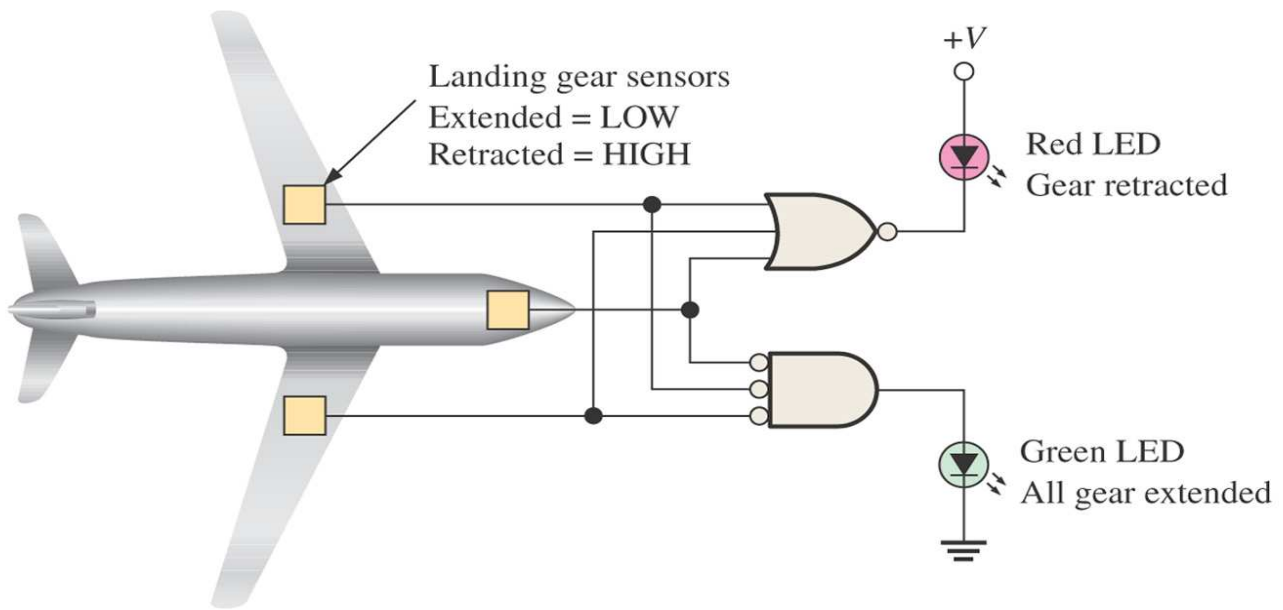


Figure 3-40

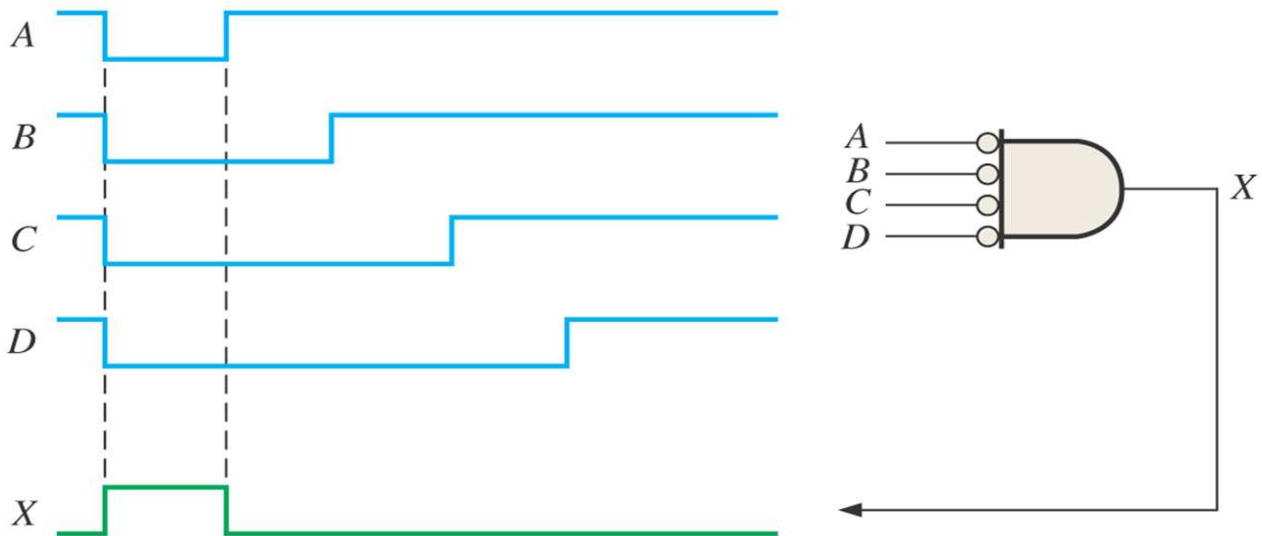
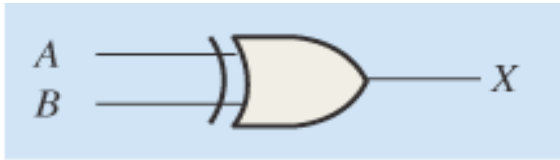
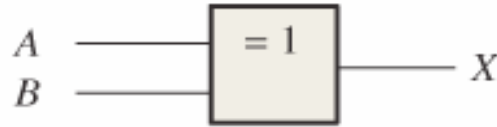


Figure 3-41 Standard logic symbols for the exclusive-OR gate.



(a) Distinctive shape



(b) Rectangular outline with the XOR

Figure 3-42 All possible logic levels for an exclusive-OR gate. Open file F03-42 to verify XOR gate operation.

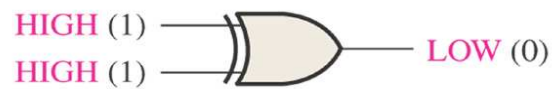
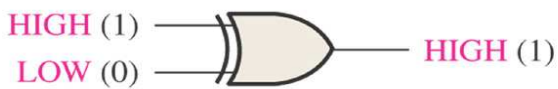


Figure 3-43

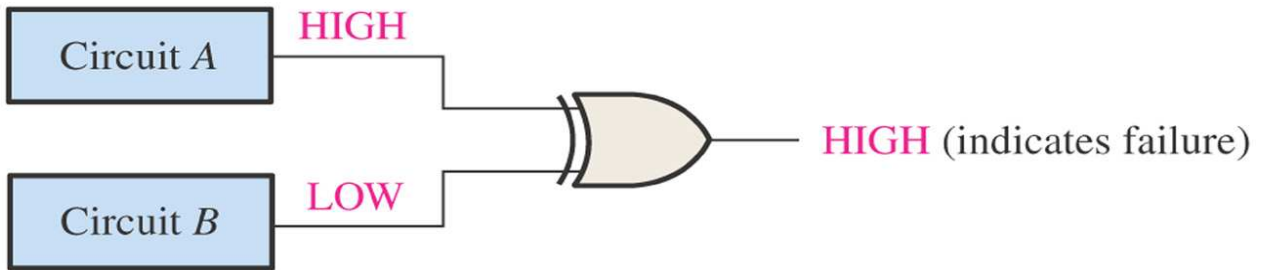
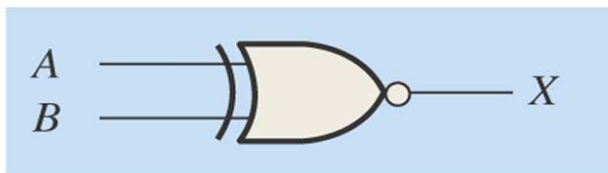
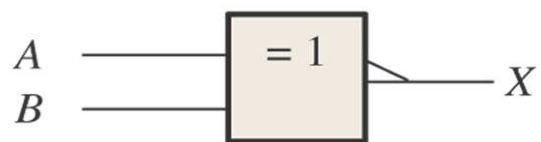


Figure 3-44 Standard logic symbols for the exclusive-NOR gate.



(a) Distinctive shape



(b) Rectangular outline

Figure 3-45 All possible logic levels for an exclusive-NOR gate. Open file F03-45 to verify XNOR gate operation.

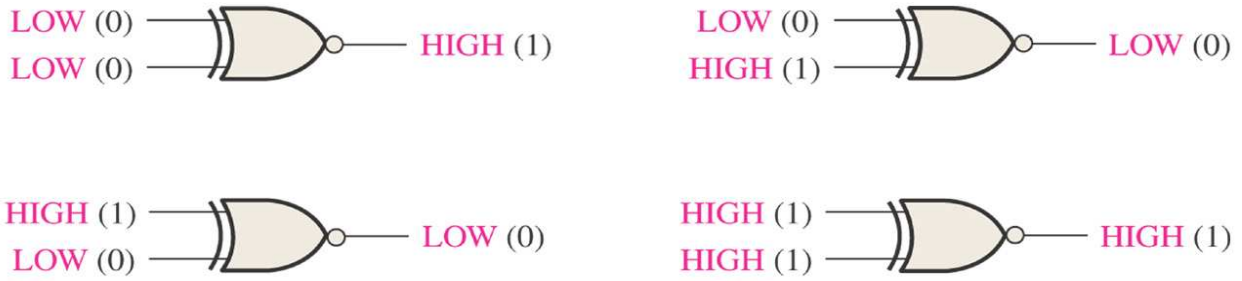


Figure 3-46 Example of exclusive-OR gate operation with pulse waveform inputs.

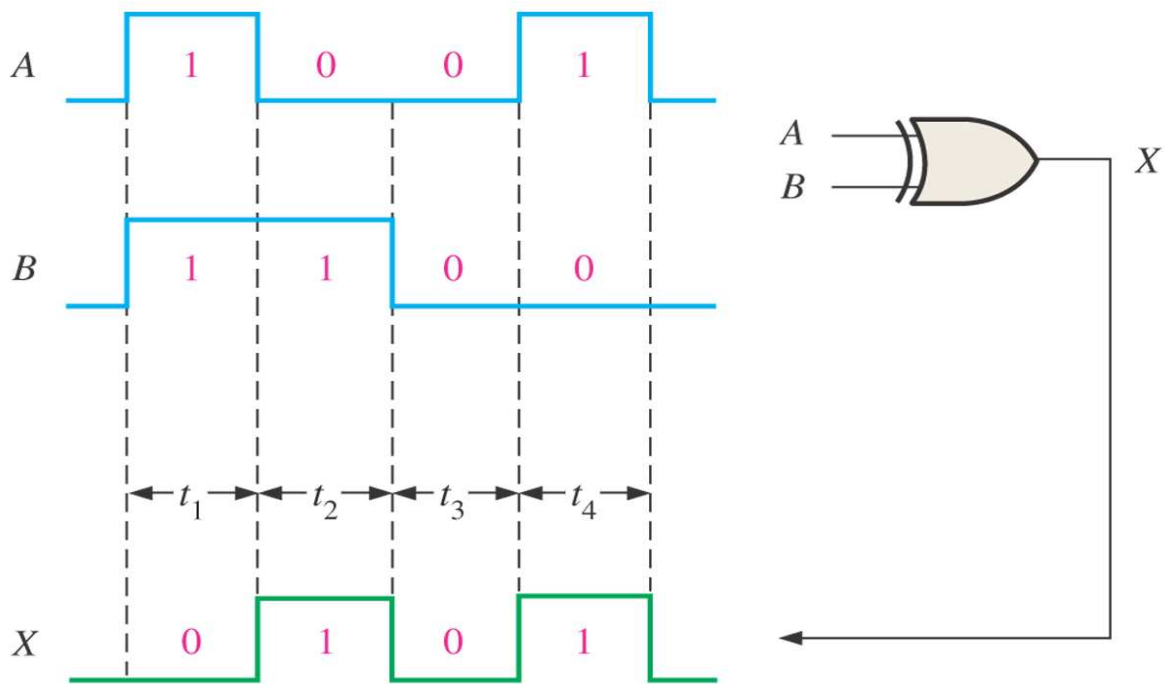
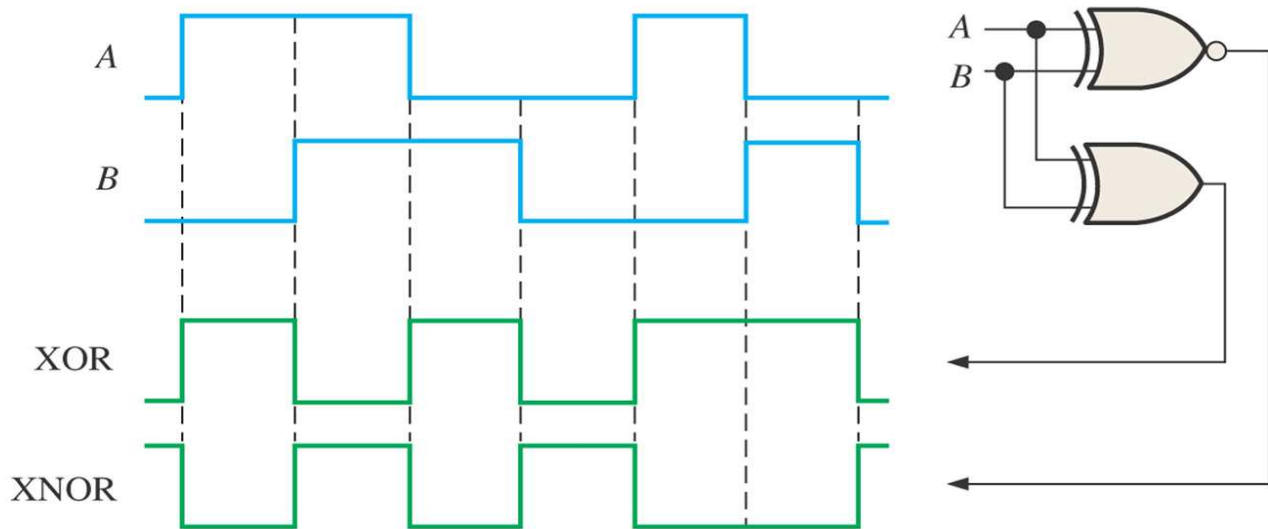


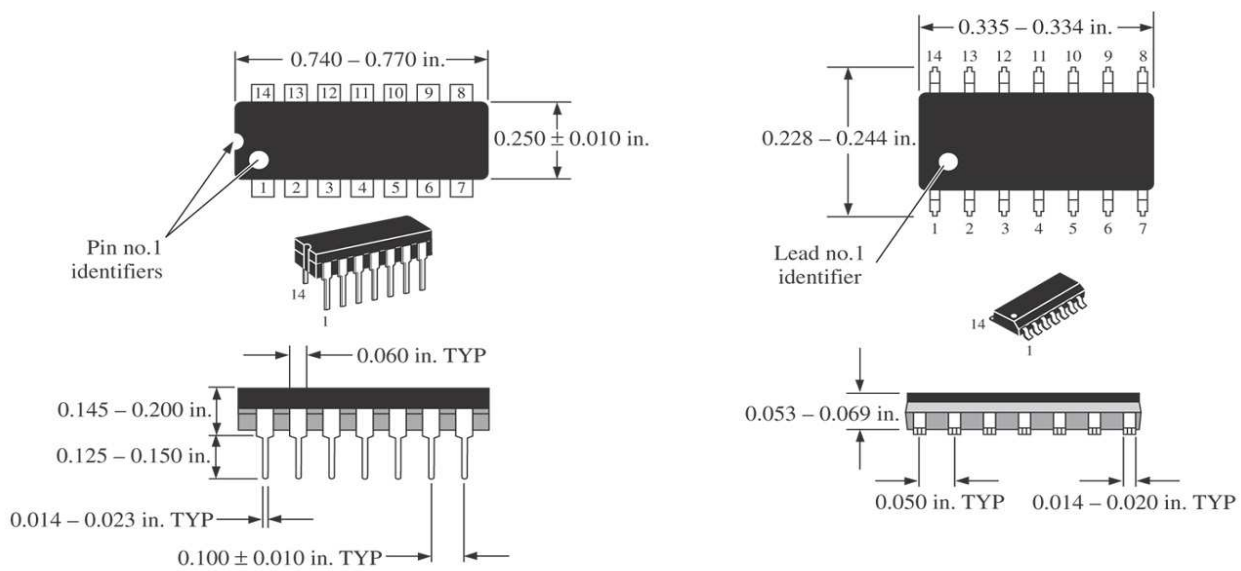
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Figure 3-60 Typical dual in-line (DIP) and small-outline (SOIC) packages showing pin numbers and basic dimensions.



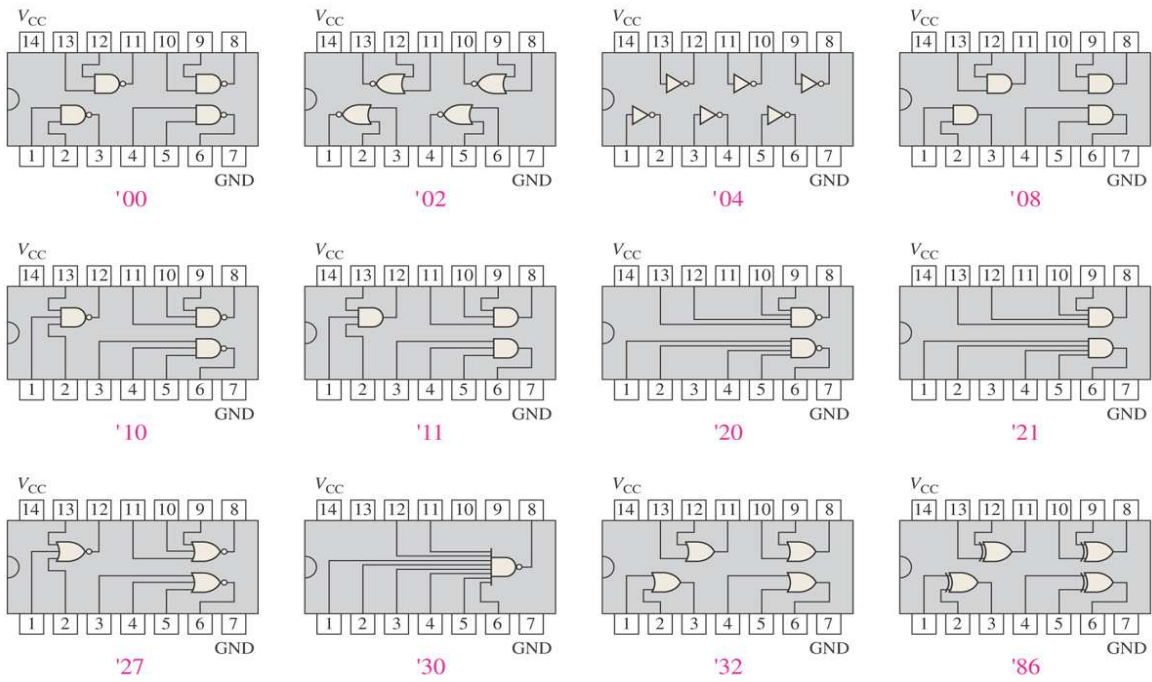
(a) 14-pin dual in-line package (DIP) for feedthrough mounting

(b) 14-pin small outline package (SOIC) for surface mounting

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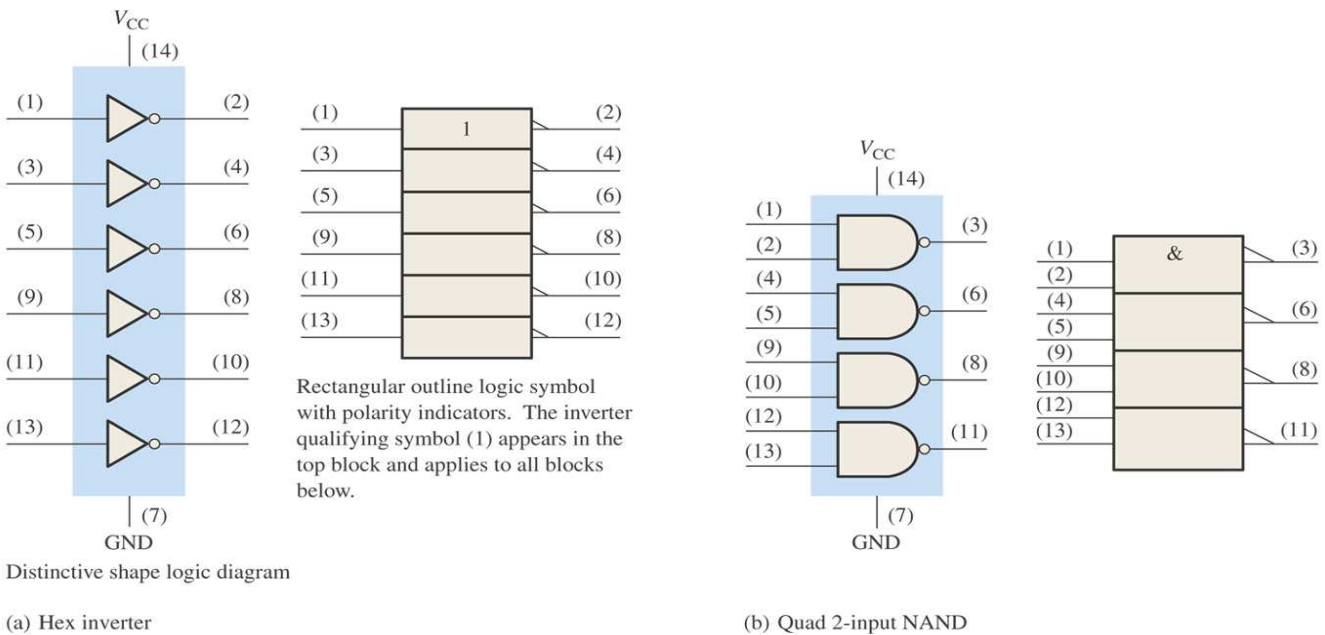
Figure 3-61 Pin configuration diagrams for some common fixed-function IC gate configurations.



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Figure 3-62 Logic symbols for hex inverter (04 suffix) and quad 2-input NAND (00 suffix). The symbol applies to the same device in any CMOS or TTL series.



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